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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,373	07/01/2003	Wee-Kuan Gan	4413-0113P	1209

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EXAMINER

RUTZ, JARED IAN

ART UNIT	PAPER NUMBER
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2187

DATE MAILED: 07/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

87

Office Action Summary

Application No.

10/609,373

Applicant(s)

GAN ET AL.

Examiner

Jared I. Rutz

Art Unit

2187

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 01 July 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-5 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-5 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 01 July 2003 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Claims 1-5, as received on 7/01/2003, are pending in the instant application. Of these, there is 1 independent claim and 4 dependent claims.

Drawings

1. The drawings are objected to because they contain multiple reference numbers that do not clearly indicate what they are associated with. For example in figure 4 item 4-1 points to a block which is also labeled 4-11, 4-2 points into a block labeled 4-21, 4-3 points into a block labeled 4-31, items 4-4 and 4-5 share the same pointer into a block labeled 4-42 and 4-41. In figure 6A item 6-120 points to the number 6-10, which is not clearly associated with anything. In figure 7, item 460 is not a step as it lacks a verb, and thus does not belong in a flowchart. In figure 8 item 510, determined is misspelled and the step also does not indicate what is determined to be CHS or LBA. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the

Art Unit: 2187

remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: The disclosure is replete with awkward phrasing which makes the meaning difficult to discern. Two examples follow.

a. "The method of the present invention can be suitably applied in any hosting device comprised of a portable ROM, a card reader in USB1.1 series, or a portable ROM, a card reader in USB2.0 series, or an IDE/PCMCIA interface."

(page 1 lines 8-11) The examiner is unsure why a portable ROM appears twice, and also of the significance of the use of the word "or" in only two of the listed elements.

b. "The controller defines the physical block that corresponds to the logical block as the mother block, then unify the mother block with the corresponding logical block wherein the back up logical zone, if the host is going to write to page N, the controller will move from block 0 to block N-1 from the mother block to the child block; then begins to write from block N of the child block." (page 5 lines 18-21) The examiner is uncertain of the meaning of "then unify the mother block

with the corresponding logical block wherein the back up logical zone", and also why N is referred to as both a page and a block.

3. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. **Claim 4** is rejected under 35 U.S.C. 112, first paragraph, because the specification, while being enabling for four 64 MB flash memory cells divided into four zones, does not reasonably provide enablement for a 64 MB flash memory cell divided into four zones and four 64 MB flash memory cells comprising four zones. The specification does not enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make the invention commensurate in scope with these claims.

6. Although this claim is fairly narrow in scope and the use of interleaving in memory is well known, it is not common in the art to use flash memories having different block sizes in the same device. One of ordinary skill in the art would be able to understand how the invention would be implemented using two or four 64 MB flash

memory divided as described in claim 4, but as disclosed the use of a single 64 MB cell divided into four zones and four 64 MB cells also divided into four zones having a different number of pages per block than the single cell would require an undue amount of experimentation to implement.

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. **Claim 3** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The meaning of the phrase "said mother and child structure possessing two physical features constitute one logical address," does not particularly point out what is meant by "two physical features." Additionally, it is unclear if the mother and child each possess two physical features, or if they share two physical features, or if between the two of them there are two physical features. Page 5 lines 16-17 state that the mother and child "are two physical features", and Page 15 lines 1-5 states that "the controller has to judge which one of these two physical positions belongs to the mother and which one of these two physical positions belongs to the child."

9. For the purpose of providing a thorough examination of the instant application, the examiner will assume that "two physical features" in claim 3 should read "two physical addresses."

Art Unit: 2187

10. **Claim 4** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The examiner is uncertain of the meaning of the phrase "correspondingly using copy back command." There is no example given of the individual flash memory cells communicating their use of a copy back command between the cells of the invention.

11. For the purpose of providing a thorough examination of the instant application, the examiner will assume that the meaning of "correspondingly using copy back command" in claim 4 is that the cells are of a type that has a copy back command.

Claim Rejections - 35 USC § 102

12. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

13. **Claims 1-2 and 5** are rejected under 35 U.S.C. 102(b) as being anticipated by Heiberger et al (US 5,341,489).

14. **Claim 1** is taught by Heiberger as:

c. An interleaving management method for upgrading a data processing speed of a flash memory, comprising a plurality of flash memory cells. See column 2 lines 59-65.

d. Wherein each of said flash memory cells comprises a plurality of blocks for reading and writing data and a plurality of pages in each said blocks.

Typically in flash memory, a block is the smallest set of erasable memory, and a page is the smallest set of data that is written in a single operation. See column 5 lines 58-63 which states that on some devices erasure is performed on a substantial portion of a flash memory, which shows that there are multiple blocks. See also figure 7 and column 7 lines 61-66, which shows multiple bytes in each block. In the given illustration of the invention there is only one block for each memory device, however it is shown (column 5 lines 58-63) that the invention can also be used with memory devices having multiple erasure blocks.

e. Continuously writing data into said plurality of flash memory cells, wherein when writing two or more sets of sectors into said plurality of flash memory cells, write a first sector into a first flash memory cell, and while the process of writing said first sector into said first flash memory cell is ongoing, a second flash memory cell is enabled so that a second sector can be written into said second flash memory cell. See column 3 lines 1-4, which state that data is latched in sequence and programmed in tandem. Figure 8 illustrates this operation. The first page is latched into the first memory device, and while it is being written, data is latched into a second memory device. Latching data into the second memory device enables the second memory device to record the data.

15. **Claim 2** is taught by Heiberger as:

f. Wherein said a plurality of flash memory cells for writing data continuously are arranged in an interleave structure. See figure 1, which illustrates the arrangement of the memory cells for the interleaving method of the invention.

16. **Claim 5** is taught by Heiberger as:

g. Wherein said interleaving management method for managing data processing of a plurality of flash memory cells is suitably applied in a hosting device, wherein said hosting device comprises, a portable ROM, a card reader in USB1.1 series, or a portable ROM, card reader in USB2.0 series or an IDE/PCMCIA interface. See column 3 lines 50-56, which show that the interleaving system is used in a memory card, and column 3 lines 65-86 which show that the card is removable.

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

18. **Claim 3** is rejected under 35 U.S.C. 103(a) as being unpatentable over Heiberger in view of Pua et al (US 2002/0147882).

h. Heiberger discloses a memory interleaving method as described with respect to claim 1 above.

- i. Heiberger does not disclose the use of the memory cells in a mother and child structure, where the mother and child have different physical addresses but share a logical address so that for writing data, transferring and erasing steps in said flash memory cells can be avoided.
- j. Pua discloses the use of a mother and child structure for writing to areas of memory that have previously been written to. See paragraphs 0033 – 0039, which show the use of the mother and child structure. Specifically note paragraph 0033, which shows that the mother and child blocks are given the same logical address.
- k. Heiberger and Pua are analogous art because they are from the same field of endeavor, namely the design of portable flash memory based storage devices.
- l. At the time of the invention it would have been obvious to a person of ordinary skill in the art to use the overwrite method disclosed by Pua in a memory card using the interleaving structure of Heiberger. The motivation for doing so would be to extend the life of the flash memory cells (see paragraph 0029 of Pua). Additionally, a stated limitation of Heiberger is that deleting a set of data corresponding to a single image that is spread over multiple blocks would require erasing all the blocks. The use of Pua's copy technique would allow the data in the blocks to be deleted to be easily saved within the memory device.
- m. Therefore it would have been obvious to combine Pua with Heiberger for the benefits of extending the life of the flash memory and easily deleting an

image without deleting other images stored in the same blocks to obtain the invention as specified in claim 3.

19. **Claim 4** is rejected under 35 U.S.C. 103(a) as being unpatentable over Heiberger in view of Applicant's admitted prior art.

n. Heiberger discloses a memory interleaving method as shown with respect to claims 1 and 2 above. Heiberger does not disclose expressly the use of memory cells utilizing the copy back command.

o. The copy back command is identified as being known in the art in paragraph 0013 of the applicant's specification. As stated in the application, the use of memory cells incorporating a copy back command is beneficial as it allows data to be read from and written to the flash memory fewer times, which allows more efficient use of the memory.

p. As the invention disclosed by Heiberger deals with reading from and writing to flash memory, it would be obvious to one skilled in the art to use flash memory that implements the copy back command to implement the memory interleaving method disclosed by Heiberger. This would allow a more efficient use of the memory cells.

q. According to page 12 lines 19-20 of the applicant's specification, the use of two memory cells is used only as an example to illustrate the operation of the disclosed invention. The specifications of the memory cells chosen in a given implementation would be specific to the to the design needs of the implementation.

Art Unit: 2187

r. Therefore, it would have been obvious to combine the Applicant's admitted prior art with the memory interleaving method of Heiberger for the benefit of an efficient implementation of Heiberger's interleaving method to obtain the invention as specified in claim 4.

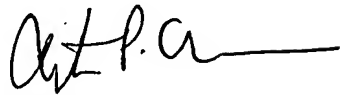
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jared I. Rutz whose telephone number is (571) 272-5535. The examiner can normally be reached on M-F 8:00 AM - 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jared I Rutz
Examiner
Art Unit 2187


Christian P. Chace
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